Co-simulation interfaces for connecting distributed real-time simulators

RT16 - OPAL-RT User Conference

7th June, Munich

Steffen Vogel

ACS | Automation of Complex Power Systems

E.ON Energy Research Center

RWTH AACHEN UNIVERSITY

Agenda

- EON Energy Research Center
  - Institute for Automation of Complex Power Systems

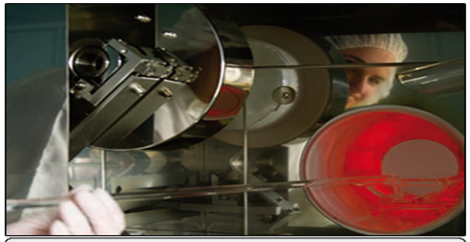
- OPAL - RTDS co-simulation Interface
  - On-going work

- Geographically-distributed simulation
  - VILLAS
    - VILLASnode / fpga
  - ERIC LAB

The E.ON Energy Research Center

- June 2006: the largest research co-operation in Europe between a private company and a university was signed
- Five new professorships in the field of energy technology were defined across 4 faculties
- Research areas: energy savings, efficiency and sustainable power sources

GGE Institute for Applied Geophysics and Geothermal Energy



PGS Institute for Power Generation and Storage Systems

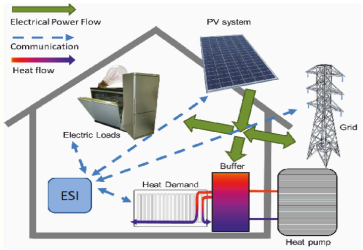
Electrical Engineering & Information Technology

Mechanical Engineering

Business and Economics

Georesources & Materials Engineering

ACS Research Areas



Applications

- Smart Cities
- Future Energy Networks
- Center for Wind Drives
- Future Internet

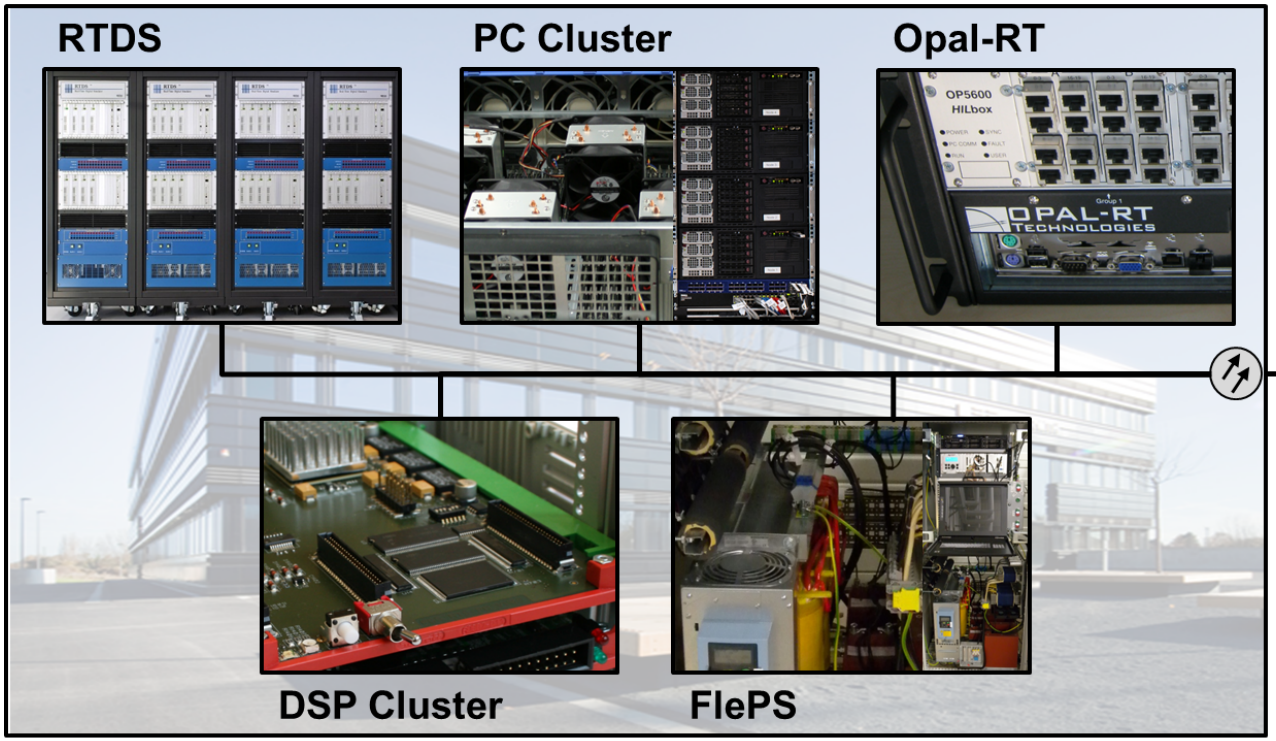
Grid Operations

- Fundamentals of Grid Dynamics
- Network Stability
- Hybrid DC/AC Networks
- Grid Monitoring
- Grid Automation
- Integration of Renewables

ICT 4 Energy

- Energy as data-driven systems
- Distributed Computing for Complex System Simulation
- Distributed Intelligence for Energy Systems
- Cloud applications for energy
- Real-Time Systems

Real Time Laboratory at ACS

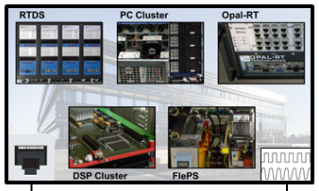


External Testing facility

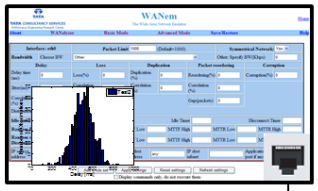
ACS Real Time Laboratory

Lab as a Network of Experiments

ACS Real Time Lab

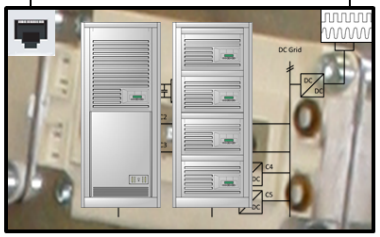


Wide Area Network Emulation



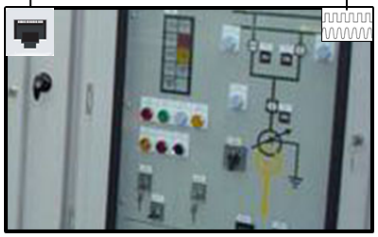
LTE for Substation control & monitoring (Ericcson)

Ethernet



Hybrid Microgrid

Phasor Measurement Units (Alstom)



Substation Automation(ABB)

OPAL – RTDS Co-simulation Interface

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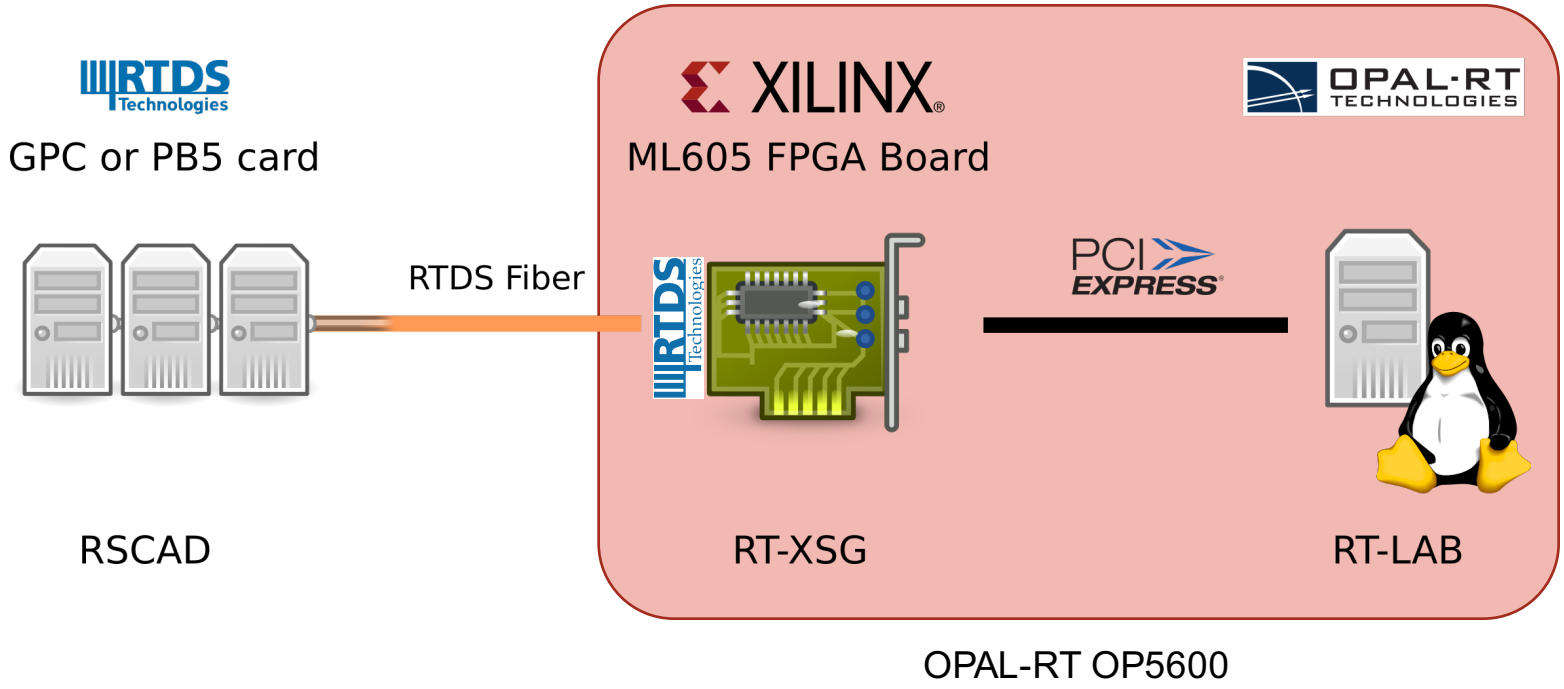
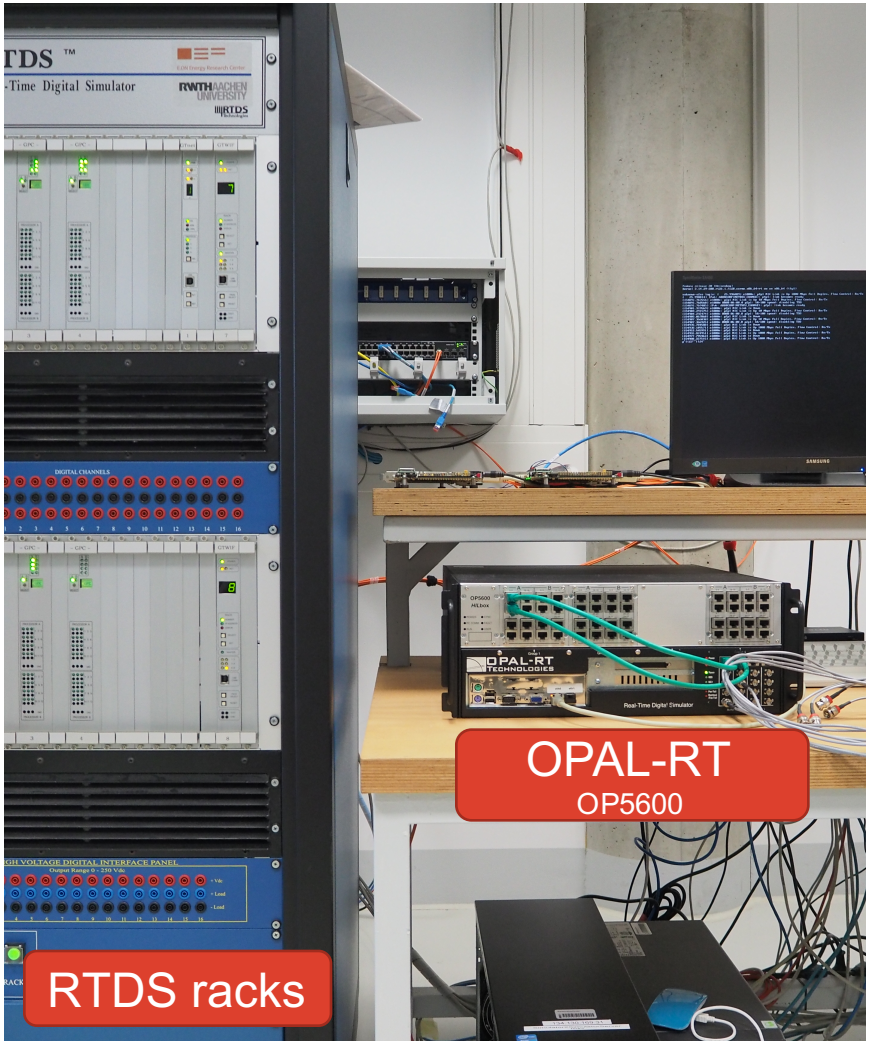
OPAL – RTDS: Overview



OPAL – RTDS: Co-simulation Interface

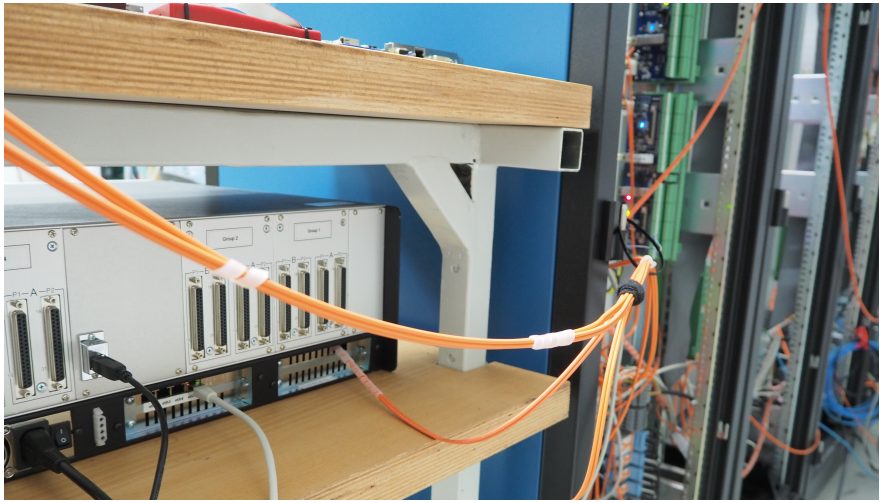
- Fully-digital coupling of two digital real-time simulators
  - OPAL-RT Technologies: OP5600: eMegaSim or HyperSim
  - RTDS Technologies: GPC / PB5 based racks
- No ADCs, DACs → No Noise & Unlimited dynamic range
  Less cabeling
- In-band synchronization
  - **1 time-step latency** between simulators
- 64x 32 bit floats or integer values per direction and TS
  - More values with multiplexing or multiple fibers
  - Small-dt mode
- Medium: Single fiber connection between
  - Xilinx ML605 FPGA board: SFP fiber module
  - GTIO peripheral port of RTDS GPC card

OPAL – RTDS: Setup



RTDS Rack next to OPAL-RT OP5600

RTDS rear panel: GPC cards

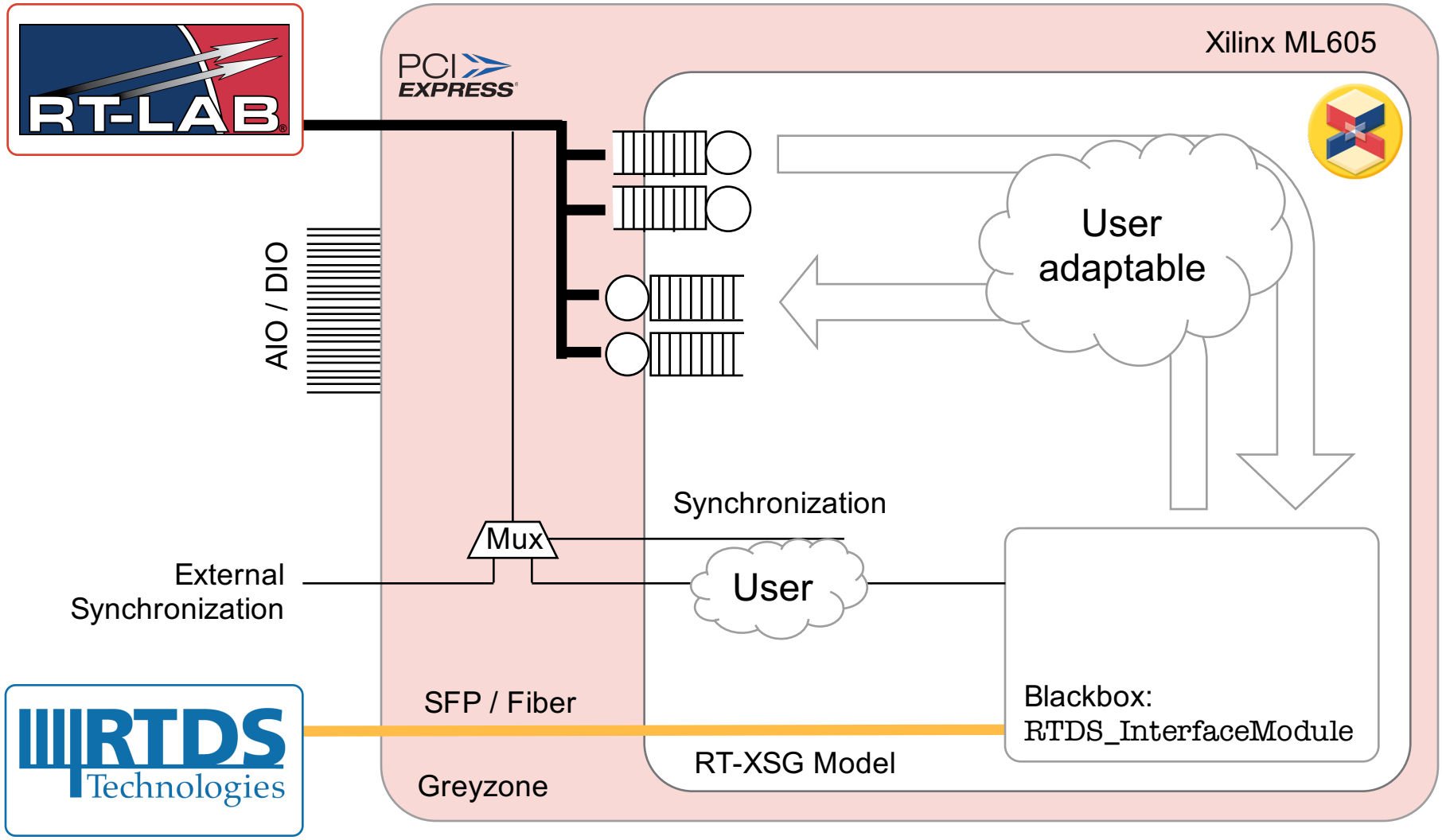


OP5600 rear panel: internal fiber connection to ML605 SFP port

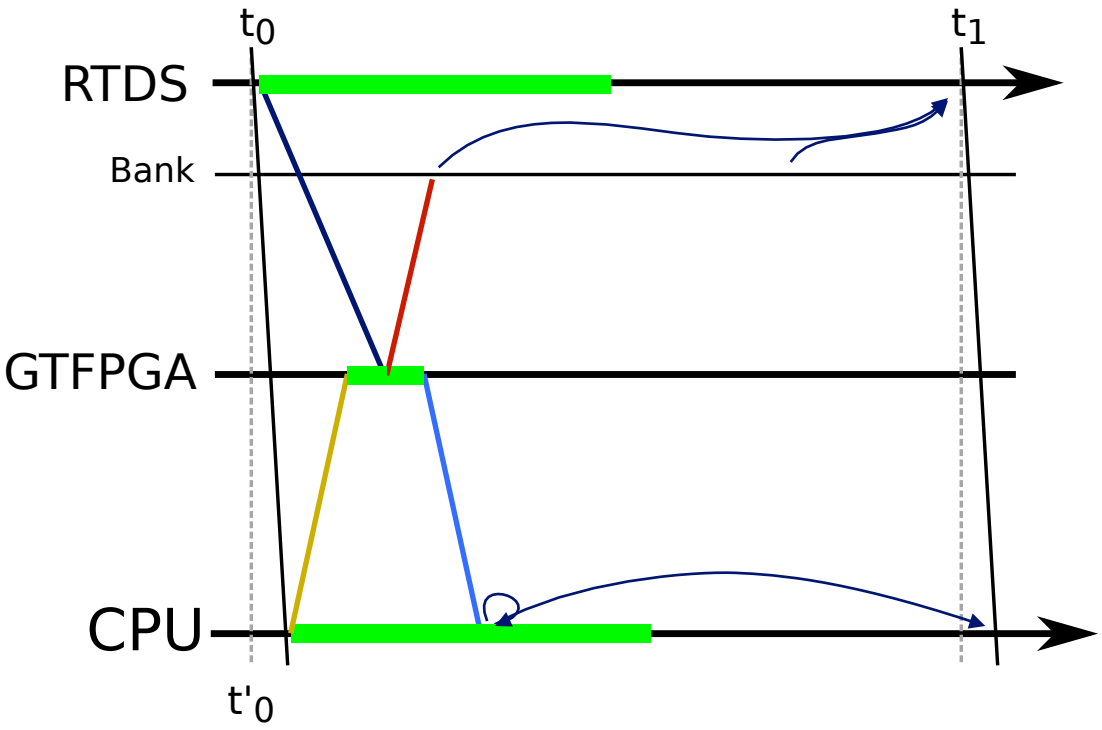
OPAL-RT – RTDS co-simulation interface

- Problem
  - RTDS is using a proprietary protocol on it‘s fibers
  - Synchronization
  - Latency
  - RTDS internal scheduling
    - Control signals vs.
    - Power System solution
- Solution
  - `RTDS_InterfaceModule` (aka. GTFPGA)
  - Synthesized FPGA netlist provided by RTDS
  - User-friendy access to proprietary interface
  - OPAL-RT can be externally synchronized by using ML605 FPGA IO‘s
  - RTDS can be externally synchronized by using GTSYNC extension module
  - Using a dedicated master clock for both
  - Transmission Line Interface (TLI)
    - Same as of inter-rack communication
  - CBuilder implementation of TLI & GTFPGA?
    - Open question...

OPAL – RTDS: RT-XSG model



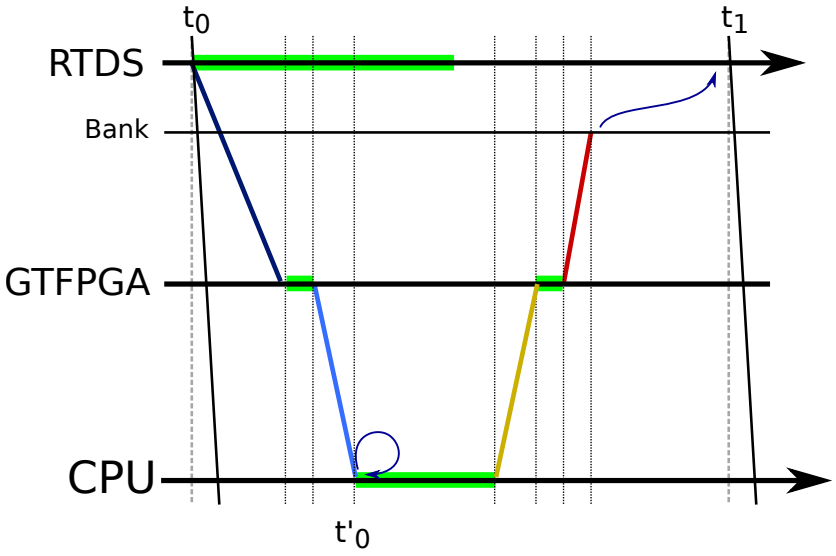
OPAL – RTDS: Timing



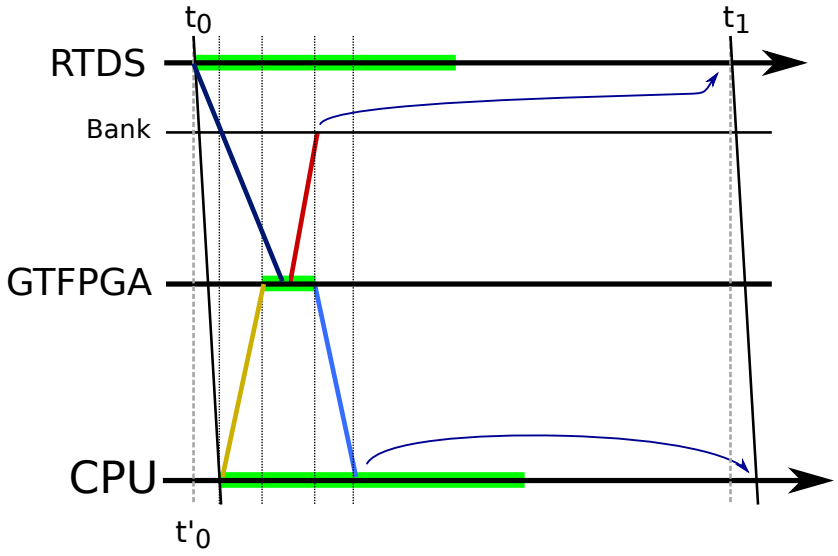
Computation

Update

OPAL – RTDS: Timing 2



(a) Serial



(a) Parallel

Computation

Update

OPAL – RTDS: Results

- **1 time-step latency** between RTDS and OPAL-RT
  - Fully deterministic: no jitter, noise or overruns
- RT-LAB simulation is **synchronized** to RTDS simulation timestep (**20 uS**)
  - Synchronization signal can be about 400 ns delayed
  - Smaller-dt possible on FPGA
- RT-XSG offers **high degree of adaptability**
  - **Multi-rate** co-simulation
  - Several scheduling schemes
- RT-LAB simulation can wait for start of RSCAD simulation case

Ongoing work

- Generic PCIe-based interface to RTDS
  - PCIe based co-simulation framework
  - VILLAS integration

- RT Co-simulation with $N > 2$ simulators

- Other clock sources for time-step synchronization
  - OPAL as master
  - Synchronizing RTDS with a GTSYNC card (PPS generated by ML605)
  - GPS / PTP IEEE 1588

Geographically-distributed simulation

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External Links

Sintef, Norway

Joint Research Center, EU

Uni. South Carolina, US

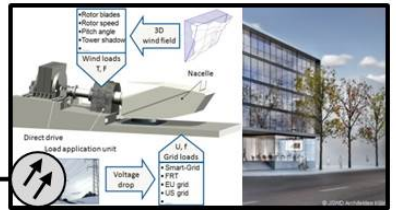
Politecnico di Turino, Italy

ACS Real Time Lab

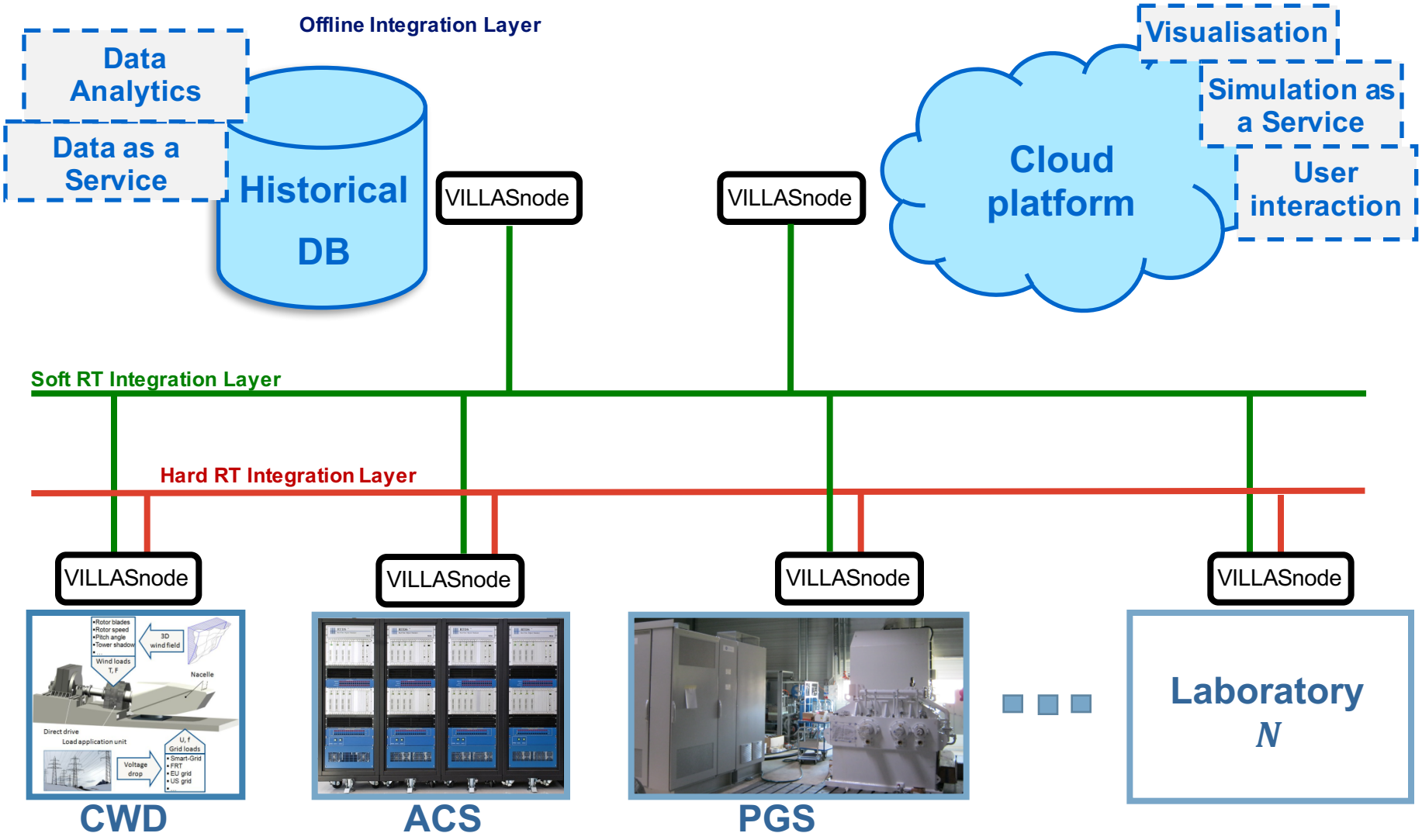
5 MW PGS Test Bench

1 MW On-Shore Wind Turbine Test Bench

4 MW On-Shore Wind Turbine Test Bench



Virtually Interconnected Laboratories for LArge systems Simulation



Geographically distributed simulation

- Co-simulation over large distances and unreliable connections

- Why
  - Share knowledge & protect IP
  - „Simulation as a Service“
  - Large-scale simulation of UCTE grid

- Network infrastructure
  - Research / university / metropolitan area networks (MAN)
  - Non-deterministic latency
  - No real-time guarantees at all

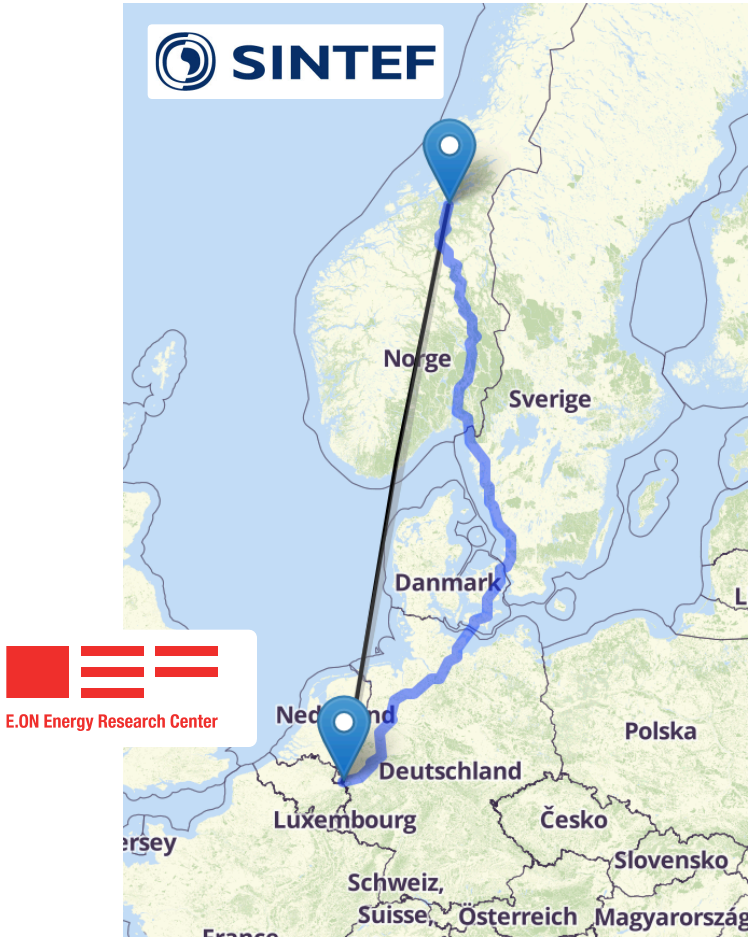
- Coupling in dynamic phasor (DP) domain
  - Latency insensitve
  - Transmission Line Interfaces based on travelling wave models

Pro Of Grids: ACS – SINTEF (Aug 2014)

- First tests between ACS in Aachen and SINTEF in Trondheim

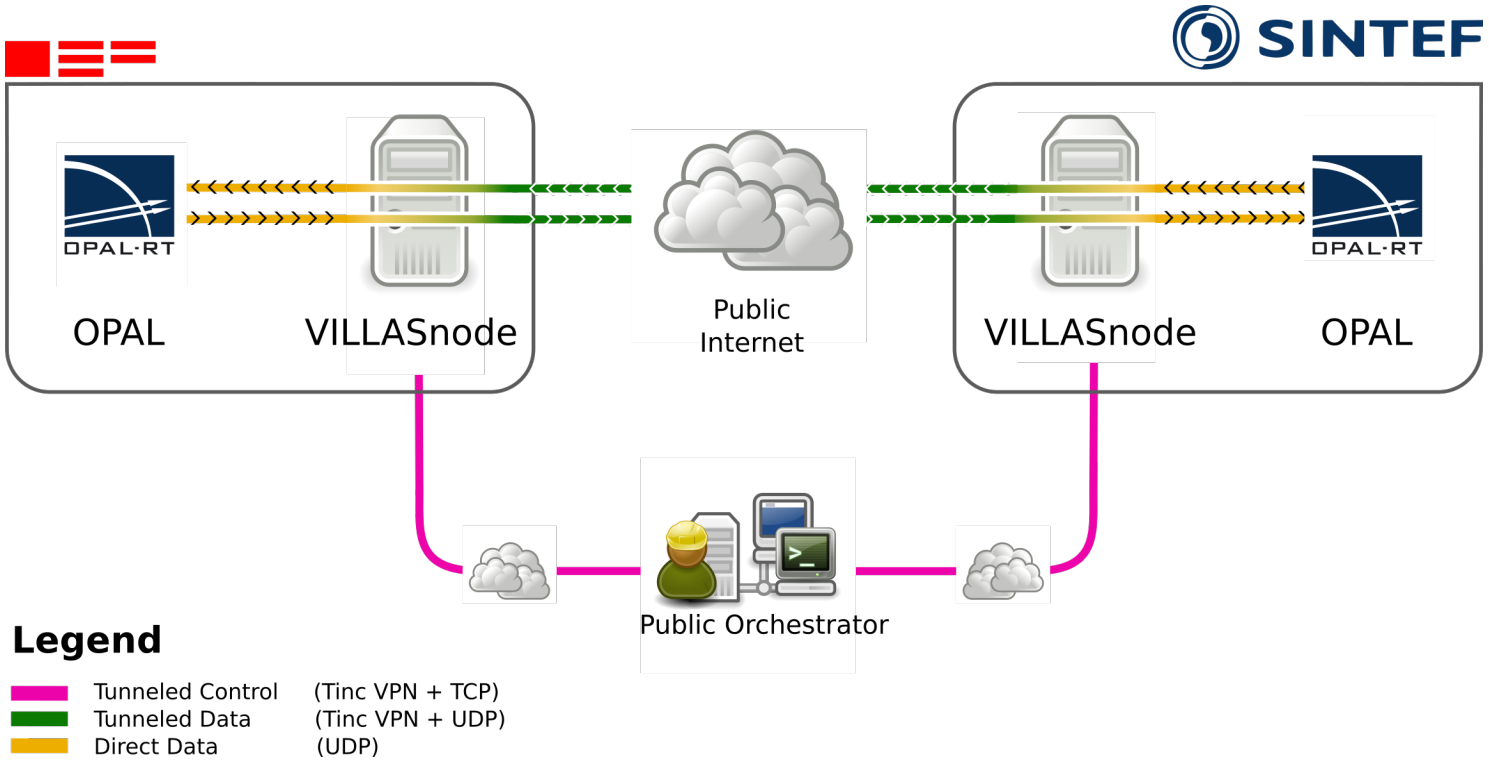
- Facts
  - Air-line distance: 1500 km
  - One-way delay: around 20-30 mS
  - Simulators: 2x OPAL-RT OP5600

- Difficulties
  - Red tape
    - Security / Firewalls
    - Software compatability
  - Non-deterministic & high network delay



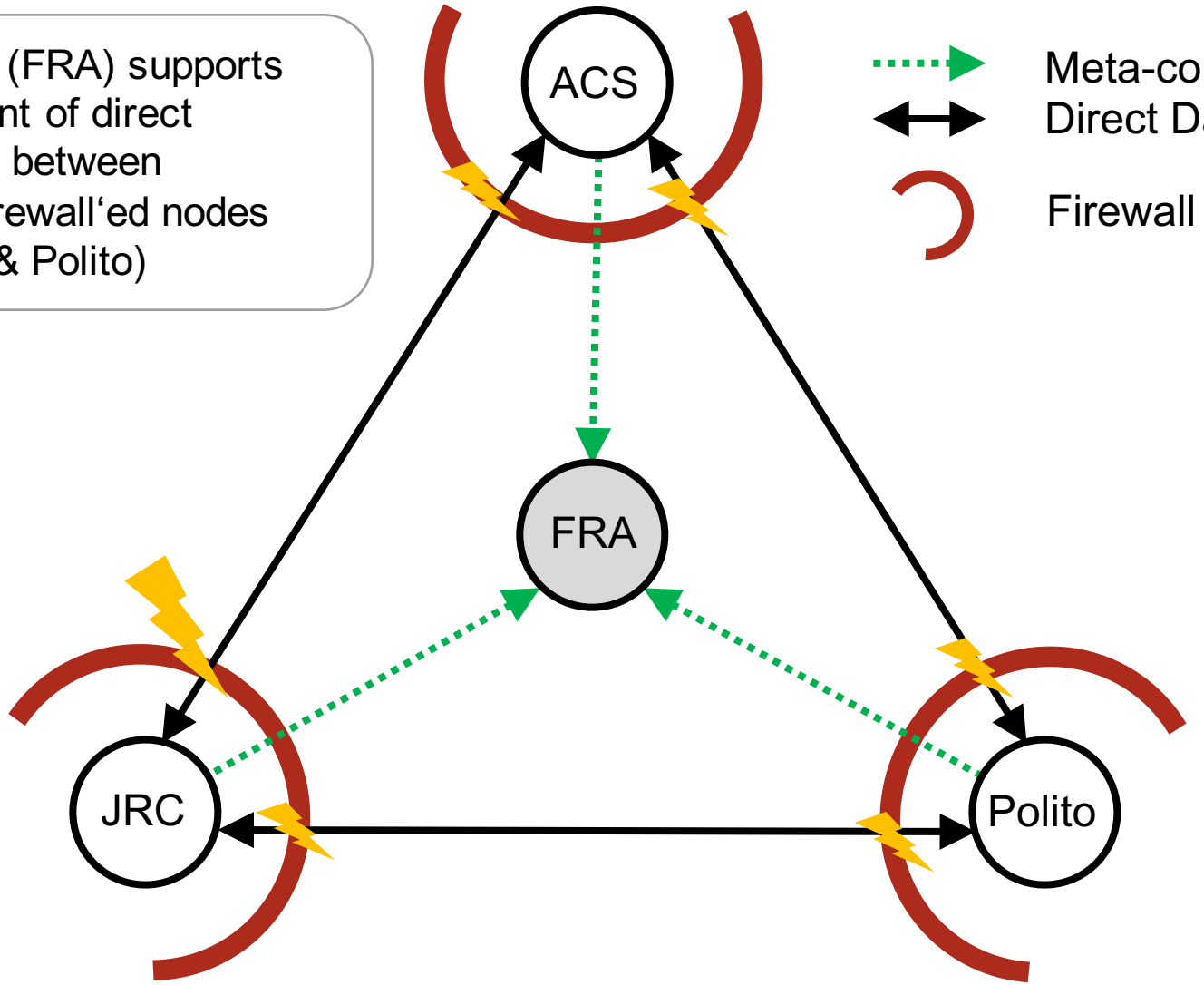
First test: Topology

- 1 VILLASnode per Lab
  - Monitoring, Statistics
  - Interface algorithms
  - VPN for Encryption
  - Local real-time co-simulation



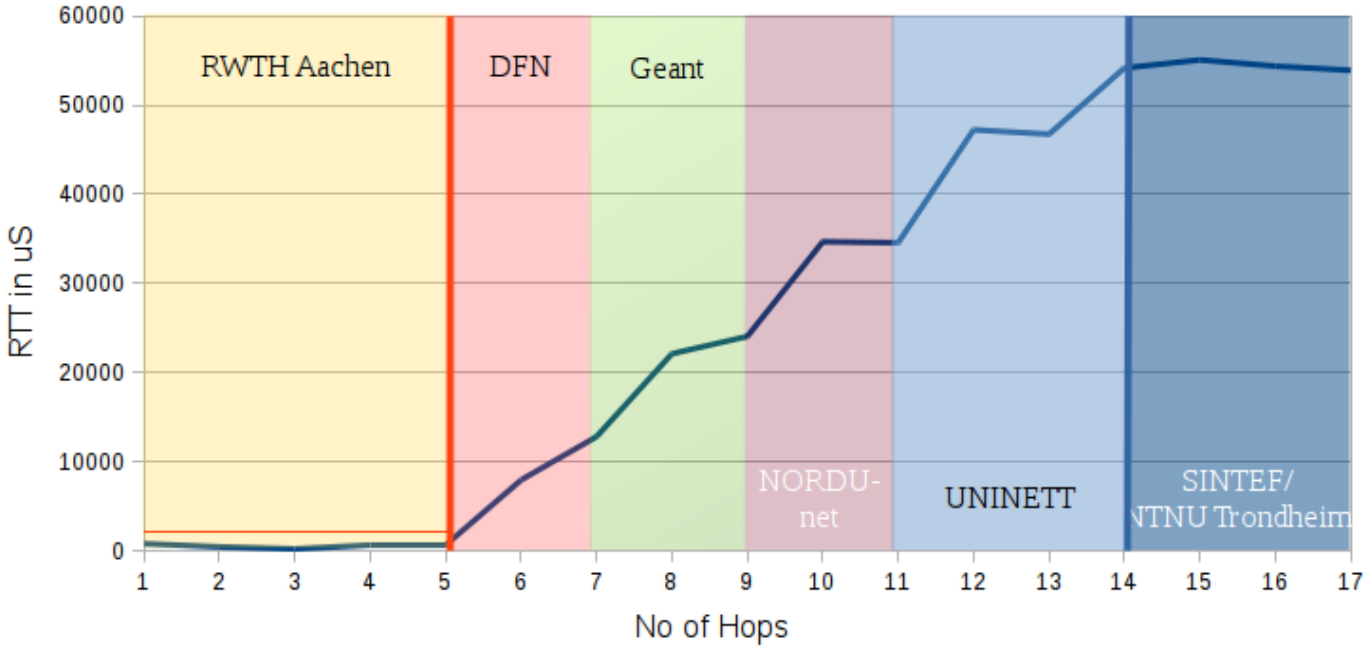
Tinc VPN: Principle & Topology

Public node (FRA) supports establishment of direct connections between otherwise firewall‘ed nodes (ACS, JRC & Polito)



Network link: ACS - SINTEF

- Mostly university & research networks:
  - RWTH, NTNU, DFN, Geant, NORDUnet, UNINETT
- Delay caused by geographical distance & congested routers
- VPN can be used to intentionally change routing
  - Can minimize delay: 55 ms => 40 ms RTT

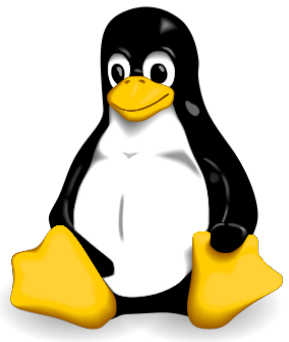


VILLASnode

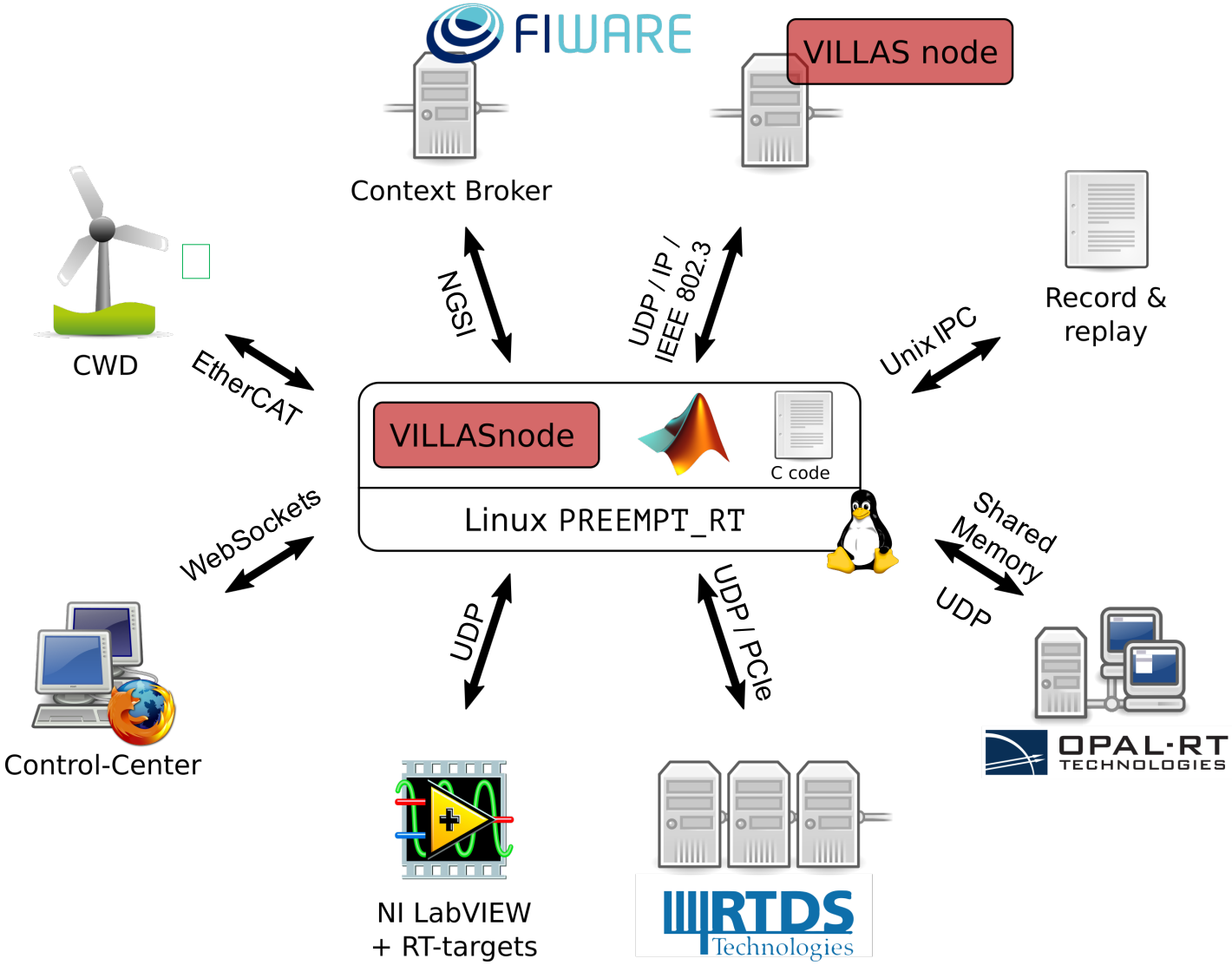
- Framework for geographically distributed co-simulation
- Acts as a gateway between a variety of different node-types
- Developed inhouse by ACS

- Object oriented **low-level C** for best performance
- Only depends on **open source** tools & libraries
- Make use of **Linux real-time** features (PREEMPT_RT patchset)
- Multi-threaded, lock-less design
- Pins pathes, nodes & IRQs to reserved CPU cores

Goals → Low & deterministic latency

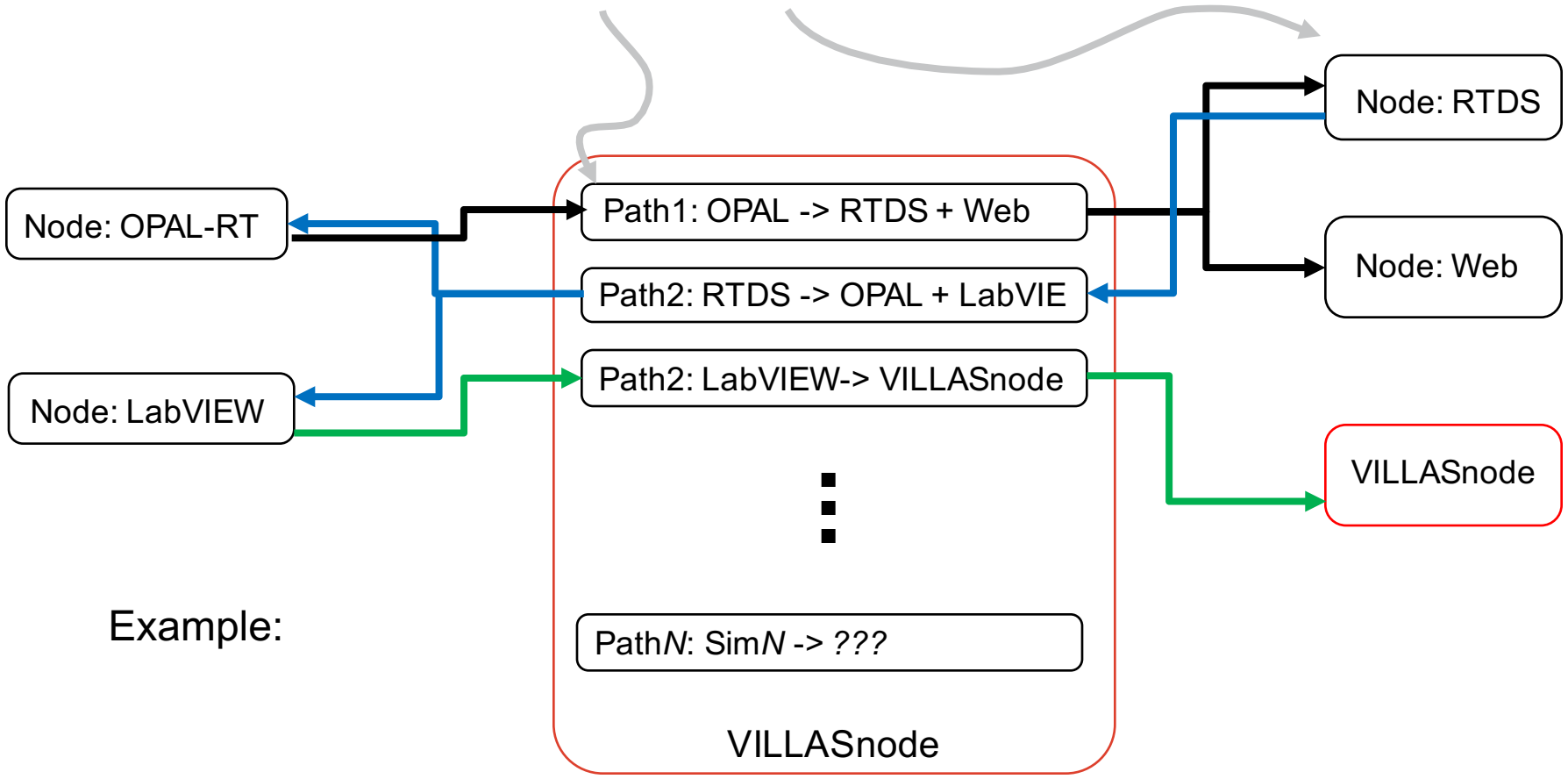


VILLASnode


FIWARE
VILLAS node
Context Broker
CWD
EtherCAT
NGSI
UDP / IP / IEEE 802.3
Unix IPC
Record & replay
VILLASnode
C code
Linux PREEMPT_RT
WebSockets
Shared Memory
UDP
UDP
UDP / PCIe
Control-Center
NI LabVIEW + RT-targets
RTDS Technologies
OPAL-RT TECHNOLOGIES

VILLASnode: Overview

- Router for sample / value based simulation data
  - **1-to-n** forwarding of sample values
  - Concept of unidirectional **paths** and **nodes**



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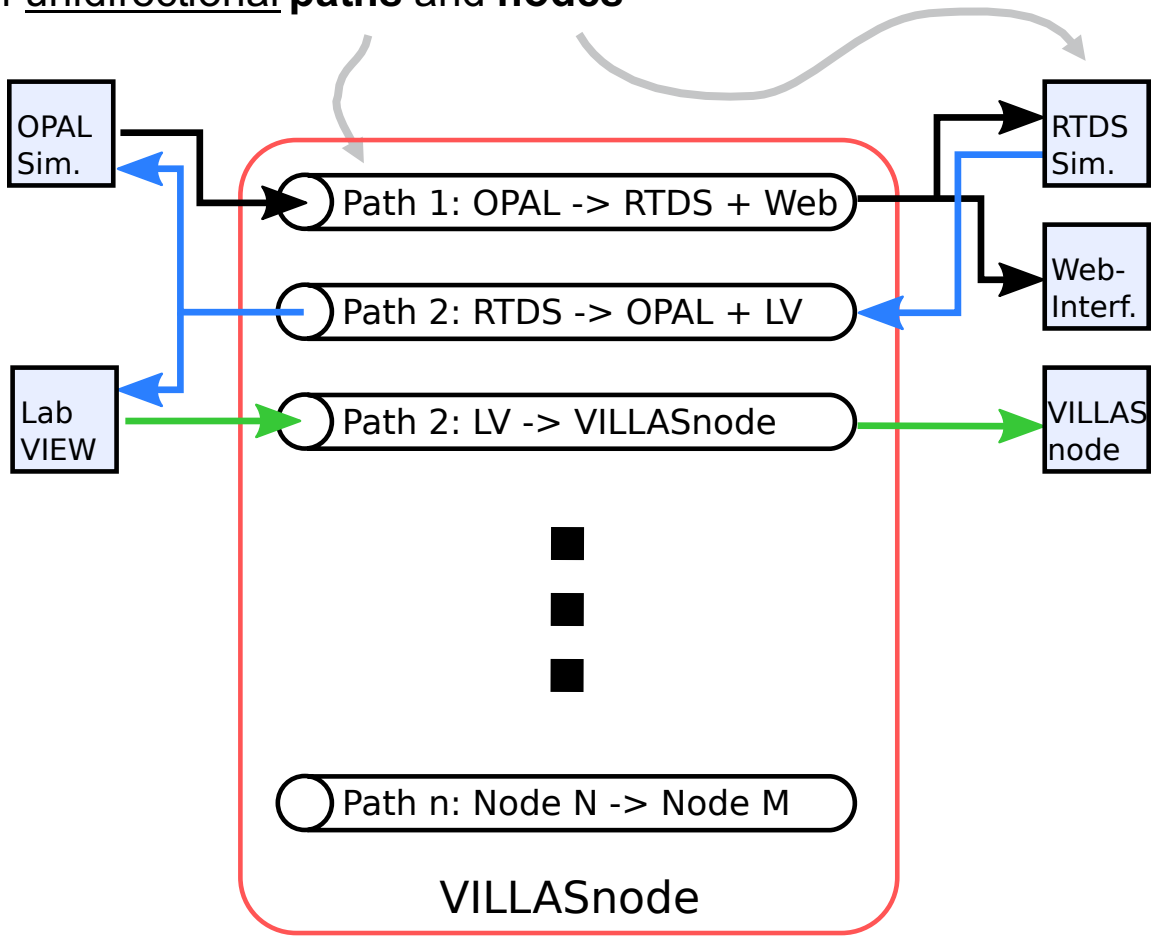
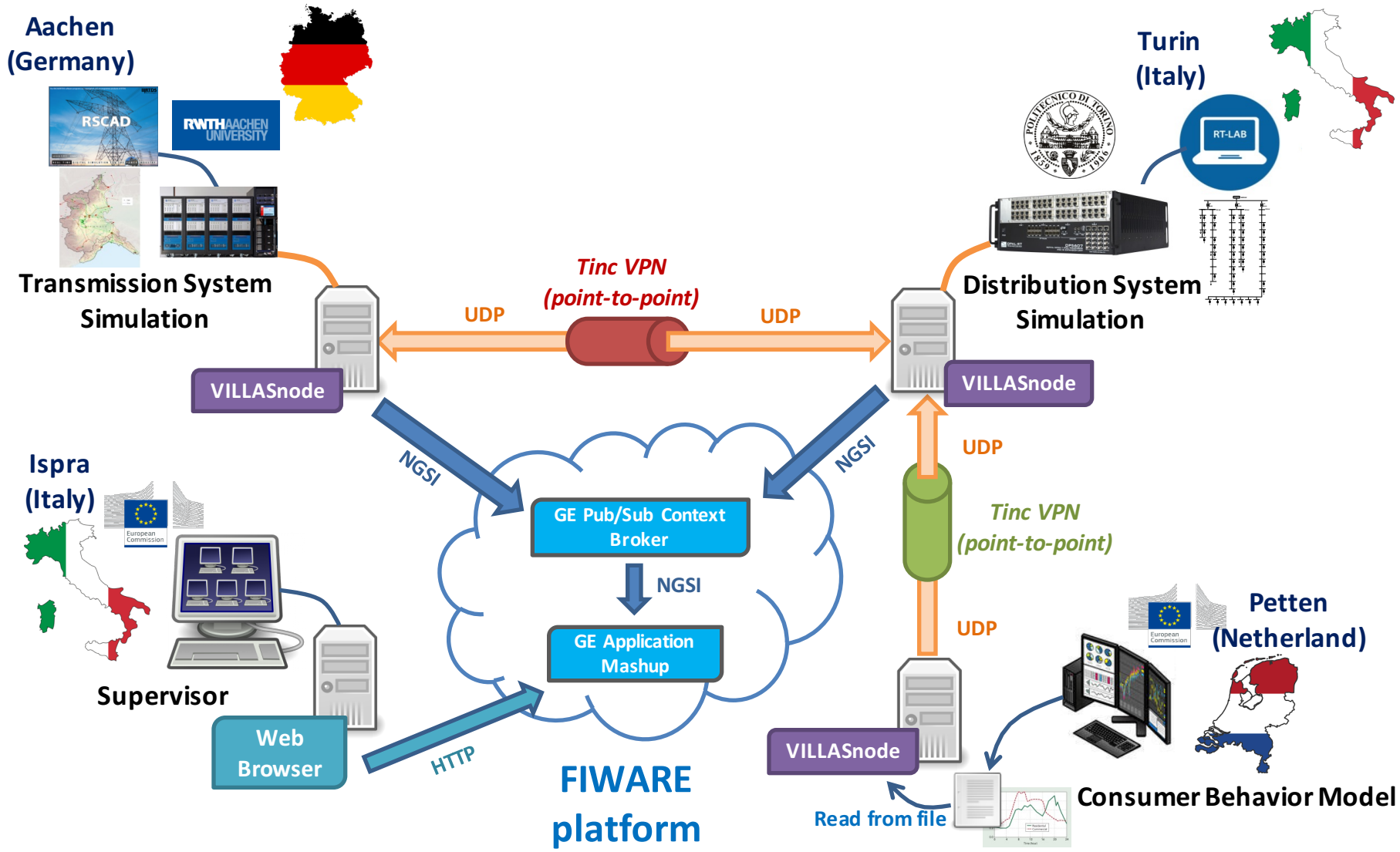
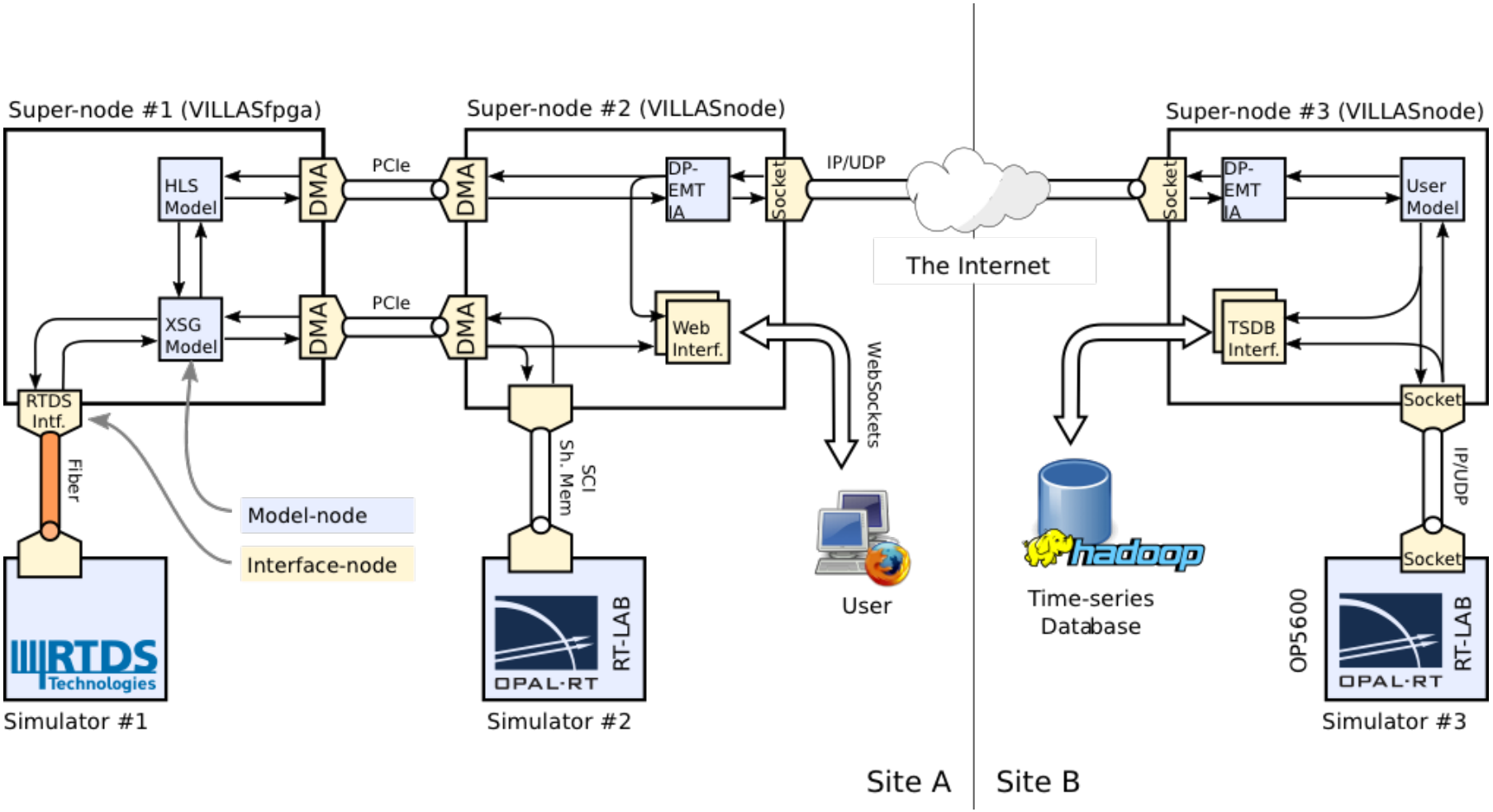


ERIC Lab Demonstration (Oct 2015)



Outlook: Combine Hard-RT Interface Layer with Soft-RT IL



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References

[1] VILLAS project

http://www.acs.eonerc.rwth-aachen.de/cms/E-ON-ERC-ACS/Forschung/Projekte/~krkg/VILLAS-Virtually-Interconnected-Labora/

[2] Tinc VPN

http://www.tinc-vpn.org

[3] OPAL-RT Press Release: RTDS-OPAL interface

http://www.opal-rt.com/press-release/eon-energy-research-center-builds-first-interface-between-opal-rt-and-rtds-technologie

[4] ERIC Lab Website

http://www.eric-lab.eu/drupal/contact

[5] JRC Technical Report: A European Platform for Distributed Real Time Modelling & Simulation of Emerging Electricity Systems

https://ec.europa.eu/jrc/en/publication/european-platform-distributed-real-time-modelling-simulation-emerging-electricity-systems

Speaker: Steffen Vogel

- Steffen Vogel is studying electrical engineering at RWTH Aachen University.
- He is currently writing his master thesis at the Institute for Automation of Complex Power Systems in the area of real-time co-simulation.
- His main focus is on computer engineering with a special interest in FPGA design.

- In 2009, privacy concerns raised by the deployment of new smart-meters lead him to start the open-source project „volkszaehler.org“ which offers everyman with insights to their unique consumer behaviour.
- His leisure time is packed with contributes to open-source projects and an addiction to running.
- After finishing his thesis, Steffen will be a future intern at OPAL-RT and looking for employment starting from April 2017.

http://www.steffenvogel.de